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A Low Offset Low Power Dynamic Latch Comparator for SAR ADC using 45nm CMOS Technology

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Abstract:ALow offset Dynamic latch Comparator using matching of input differential pair MOSFET's and a PMOS clock transistor is anticipated. The dimensions of differential pair transistors can be lessened by using Monte Carlo analysis. Experimental results show that the Dynamic comparator attains 13mV offset at a 200 KHz clock frequency and 13 KHz input frequency at a common mode and reference voltage of 0.55V, while dissipating 2.13µW. The comparator load capacitor is 217aF for reducing output delay in Successive Approximation Register (SAR) ADC. The Dynamic Latch comparator Layout has been fabricated in 45nm CMOS technology with an area of 34.0572µm^2.
Keywords: Comparator,HV_t Cell, Mismatch, Offset Voltage, Power consumption, Threshold voltage.

Introduction

Comparators have a decisive impact in many applications like ADC's, for example, Successive approximation register (SAR) ADC, Flash ADC, Memory sense amplifiers and Receivers. In the current year's attention, has been given to the design of low power and extreme speed. With these parameters offset voltage also have given the same importance. As the process technology is waning gradually, a huge amount of components can be housed on a specific chip. Nevertheless, lessening in technology consequences large offset voltage [1]. However, there are a ration of types of Comparators such as pre amplifier based comparator, dynamic latched Comparator and Open loop comparators, etc. Among those Comparators preamplifier comparators suffer from extreme power and lesser gain due to technology scaling. Therefore, dynamic comparator structures are extremely required. However, the offset voltages of such comparators are restricted. Therefore, the Offset voltage is one of the most important factor to design any Dynamic latch comparator. The important parameters for designing any comparator are current factor β, threshold voltage V_{th}, width to length ratio (W/L) and capacitive loads at the outputs. Previously, many offset cancellation techniques have been proposed [2]-[4]. In a report [5] explains the Analog Offset Calibration method intended for Biomedical SAR ADC has been proposed. In a report [6] Dynamic offset cancellation technique has been explained.

In order to understand low power, low offset for the monotonic switching arrangement of SAR ADCs [7] a dynamic comparator with offset reduction has been proposed by changing the (W/L) ratios of input differential pair and current source. Offset can be measured using simple DC analysis by changing the unique of the input source from $-V_{dd}$ to $V_{dd}$and observing the voltage at 0 V. The simulation results shows that by changing the (W/L) ratios offset voltage has reduced to 13mV at 1.1 V supply voltage which is very much desirable.

The paper is organized as follows. First describes the operation of Dynamic latch comparator. Next, describes the operation of proposed Dynamic latch comparator in terms of delay and offset. Next presentsSub threshold region concept if the MOSFET's want to operate for Low power. Next presents the measurement results and comparisons with previous works are shown, followed by conclusions.

Dynamic latch Comparator

The Dynamic latch comparator with a current source Schematic is shown in Figure-1. It works in two phases [7].i) Conversion phase ii) Regeneration phase. In Conversion phase, the input voltages of Dynamic Latch comparator approaches to the ground. When ClkC is high the MOSFET M7 is in the cut-off region, thenthe comparator outputs O_{utp} and O_{utn} are changed to high. AfterClkCdrives low, at that time the MOSFETS M5 and M6 are in the cutoff region plus M7 will be turning on. At that time, the comparator is in comparison phase, the M7 and Mb act as a constant current source and decreases the consequence of channel length modulation. Now the input differential pair M1 and M2 of the Dynamic Latch comparator, relates the two input voltages, then the latch restoration strengths one output to high and other output to low

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by two inverters. By resting the voltage V_{bias} and matching the size of Mb and M7, carefully a reduced amount of offset voltage can be realized.

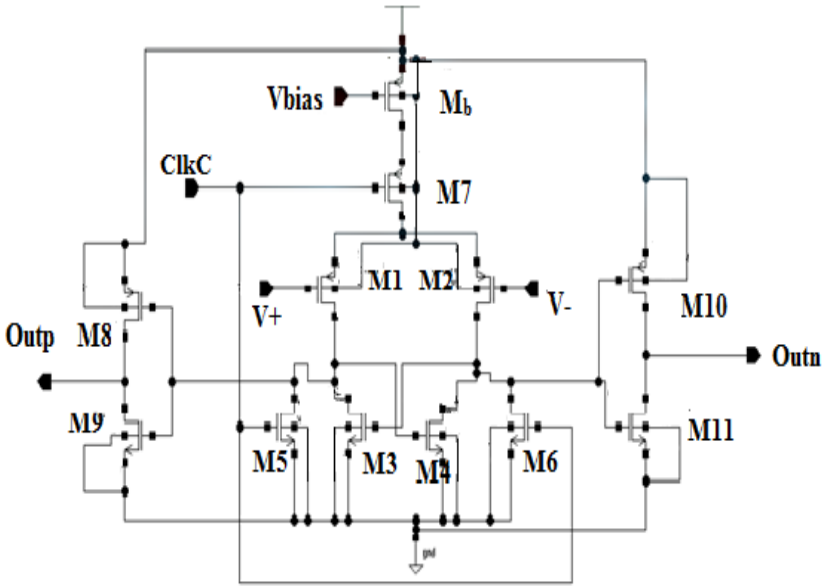

Figure 1. Conventional Dynamic latch Comparator

Proposed Dynamic latch Comparator

The Proposed comparator with reduced Width and Length ratios is shown in Figure2. The operation of the proposed dynamic comparator is same as conventional comparator. To enhance the Dynamic Latch comparator in terms of offset voltage and power, the mismatches of the differential pair has to be proved first. The PMOS transistors (M1, M2, M7, Mb) are taking the aspect ratio of W/L=4µm/180nm and NMOS transistors are taking the aspect ratio of W/L =2µm/180nm and the PMOS inverter pair (M8 and M10) aspect ratio is 3µm/180nm.The mismatch in threshold voltage $V_{th}$is $\sigma_{V_{th}} = \frac{AV_{th}}{\sqrt{WL}}$and current factorβ $= \mu_n c_{ox}$canbe expressed as$\sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$. Here, AV_{th} and $A_\beta$are process parameters [8]. The offset voltage equation [6] of the Dynamic Latch comparator can be stated as $V_{os} = \Delta V_{th\,1,2} + \frac{(V_{GS}-V_{TH})_{1,2}}{2}(\frac{\Delta M_{1,2}}{M_{1,2}} + \frac{\Delta R}{R})$ (1)

Where$\Delta V_{th1,2}$is the threshold voltage of the input differential pairM1 and M2. $(V_{GS}\text{-}V_{TH})_{1,2}$ is the effective voltage of the differential pair,$\Delta M_{1,2}/M_{1,2}$is the mismatchamong M1 and M2, ΔR is the loading resistance discrepancy persuaded by M3-M6.The first term is a change of threshold voltage, and it doesn't affect the functioning. Another term is a signal reliant on dynamic offset. The MOSFET M12 is used to reduce the mismatch between the MOSFET's M1 and M2.Mismatch parameter was reduced, to lessen the Offset voltage, and by using Monte Carlo analysis, the widths of M2 and M7 are measured as 3.68µm and 3.8µm respectively. If the Dynamic latch comparator transistor width increases then the average power consumption also increases.

The effective gate voltage of the input differential set can be condensed, nonetheless this reduces the rapidity of the process. A modest method stands to cascade a biased MOSFET (M_b) on the highest of the switch PMOS and keep the Zero DC voltage. When the common mode voltage varies M_b retains the effective gate to the source voltage of input differentialsetnearby constant value. In this situation, the delay [1] time of the comparator is specified by

$T_{delay} = t_0 + t_{latch}$ (2)

$= 2\frac{C_p V_{thn}}{I_{tail}} + \frac{C_p}{g_{m,eff}} \ln \frac{V_{dd}\, I_{tail}}{4V_{thn}\, g_{m\,1,2} \Delta V_{in}}$ (3)

$t_0$stances for a capacitive charge time tillthe cross-coupled pair M3 or M4 works. The t_{latch} signifies the latching wait time of (M3-M6)NMOS transistors. $I_{tail}$is the tail current. V_{thn} is the threshold voltage of the NMOS transistor. ΔVin is the small variation of differential voltage. The $g_{m1,2}$is the Trans conductance of the input differential pair.C_p is directly proportional to delay. So in this proposed circuit to reduce delay,

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minimum capacitor value (i.e 217aF) was placed at the output of the comparator. The minimum capacitor value was measured by Monte- Carlo analysis.

As the technology is diminishing the leakage currents are more. Because of leakage current power dissipation is high. So to use this design for low power applications, reduce the power in the Sub-threshold region. The concept is explained here.

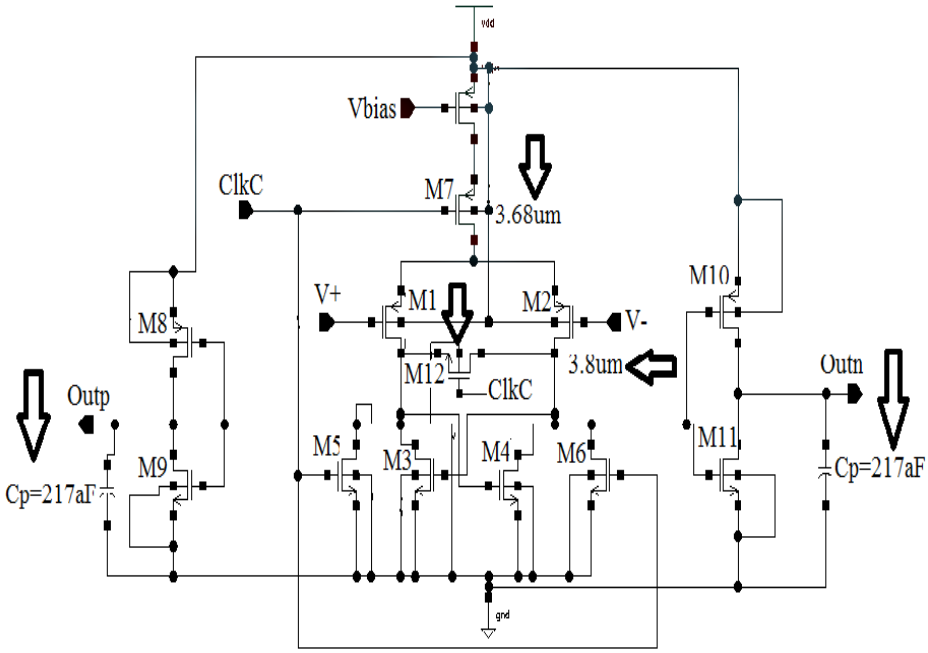

Figure 2. The Proposed Dynamic Comparator

A. Sub-Threshold Region

The region just below $V_t$of a transistor is called sub-threshold region[10]. After the gate to source voltage $V_{gs}$is less than threshold Voltage V_t, then the leakage current

$$I_{leakage} = \mu(W/L)e^{(-qV_t/\eta KT)} \quad (4)$$

Where μ = mobility
W = width of MOSFET
L = Length of MOSFET
K = Boltzmann's constant
T = Temperature
q = Charge of an electron
V_t= Threshold Voltage
η = Sub-threshold switching Coefficient

This indicates that the parameters μ, K, q are constants and only $V_t$and W are dependent on $I_{leakage}$. As the width of MOSFET rises leakage current also rises and as $V_t$increases, the leakage current decreases exponentially. This in turn lessens leakage power. So in this circuit all PMOS transistors are replaced with high V_t (HV_t)[10] cells. So the MOSFETs will be operated at their threshold voltage. Because of this delay increases and power dissipation was reduced greatly. This justifies the usage of high $V_t$devices for low power applications in our design. The simulation results after applying HV_tcells are shown in table-1.

Measurement Results

The above circuit is designed and the evaluation is done using Cadence Virtuoso in 45nm CMOS technology. The results are shown in table-1. This Dynamic Latch comparator is designed with 550mV common mode voltage and the supply voltage is 1.1V. The input and clock frequencies are 13 KHz and 200 KHz respectively.

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The results show that because of the transistor diminishing the offset voltages are very high and power consumption is very less. And while designing any comparator offset voltage should be kept within the limit and to further reduce the offset voltage MOSFET dimensions are increased to 4um and 3um respectively as shown in figure-I. Because of this power was increased and offset voltages are reduced from 505.97mV to 114mV as shown in figure. 3.

Table 1: Performance of Dynamic Comparator

Parameter	**In45nmTechnology**	**Increasing W/L ratios**	**Proper sizingof MOSFETS For reducing threshold mismatch**	**Applying HV_tconcept**
Power(W)	65.15n	2.511µ	2.131µ	265.3n
Delay(S)	474n	338.75n	342.9n	571.8n
Offset(V)	505.97m	114.79m	22.01m	462m

Even though this is a big value. The fingers of the MOSFET are accurately sized for reducing the offset voltage. Then the offset voltage is reduced to 22mV as shown in figure. 4. The obtained offset voltage can be tolerable and still further reducing the offset voltage, adjust the threshold voltages by Monte-carlo analysis.

Table 2: Performance of Dynamic Comparator

Width of MOSFET (M2)µm	**Offset(mV)**
3.6578	12.4
3.642	18.154
3.626	19.566
3.6105	20.198
3.68	13.0

The analysis was done for the PMOS differential pair and Clocked PMOS(M7), then the widths of MOSFETS are adjusted to 3.8um and 3.68um respectively.The MOSFET M12 is used to reduce the mismatch between the MOSFET's M1 and M2 and after sizing the input differential pair, the offset voltage was reduced to 13mV as shown in figure. 5. For different Widths of the input differential pair and corresponding offset voltages are shown in Table-2.

Theproposed Dynamic Latch comparator delay is condensed from 474nS to 338.75nS as shown in table-1. After reducing the threshold mismatches the delay was slightly increased to 342.9nSas shown in table-1. After applying the HV_tconcept to the comparator delay is increased to 571.8nS.

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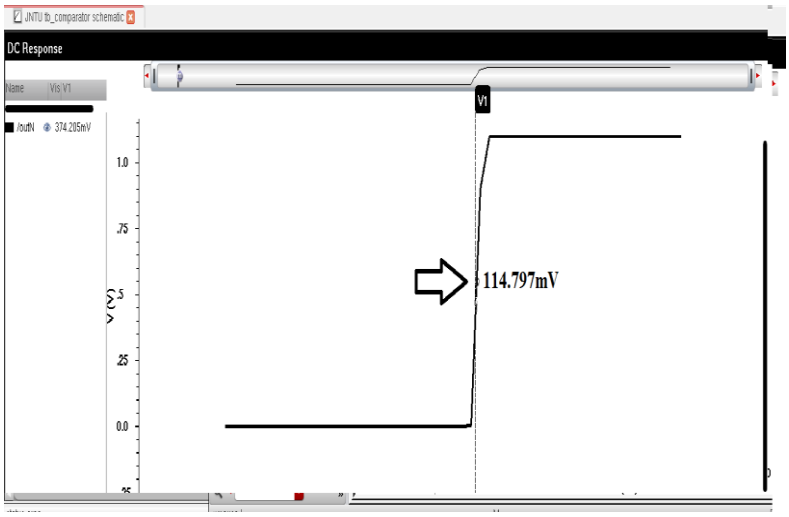

Figure 3. Offset voltage waveform before matching the threshold Voltage

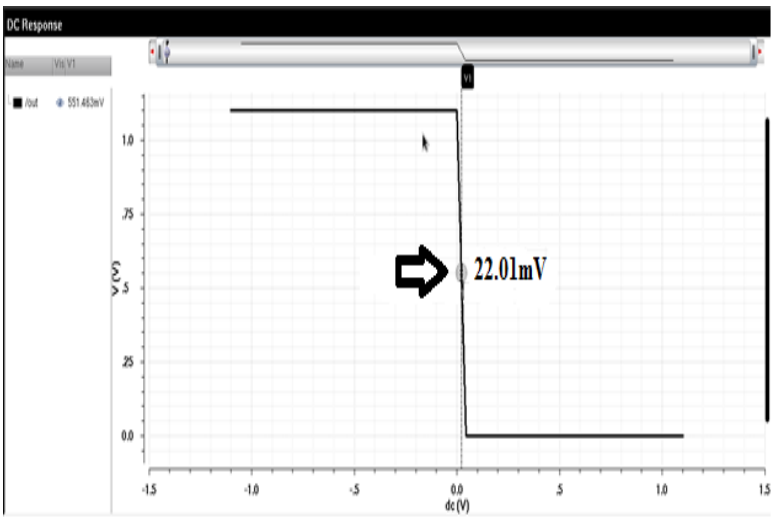

Figure 4. Offset voltage reduction after matching the MOSFETS

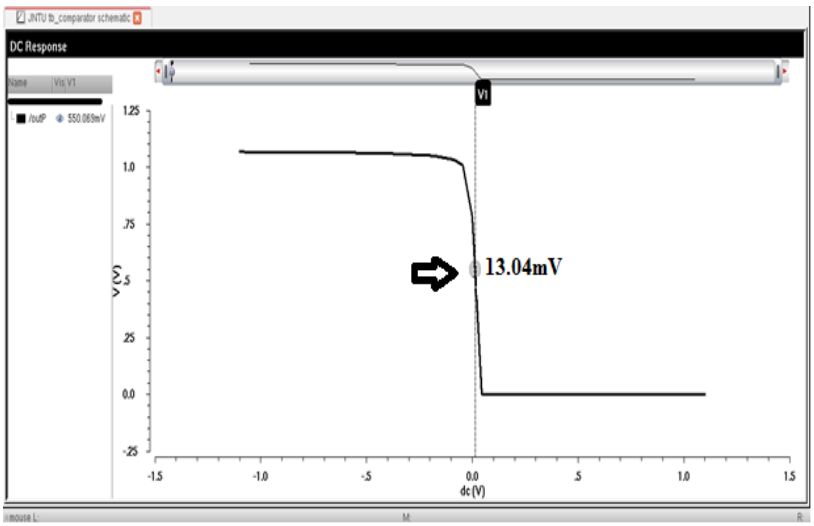

Figure 5. Offset voltage reduction after proper sizing of the MOSFET M2

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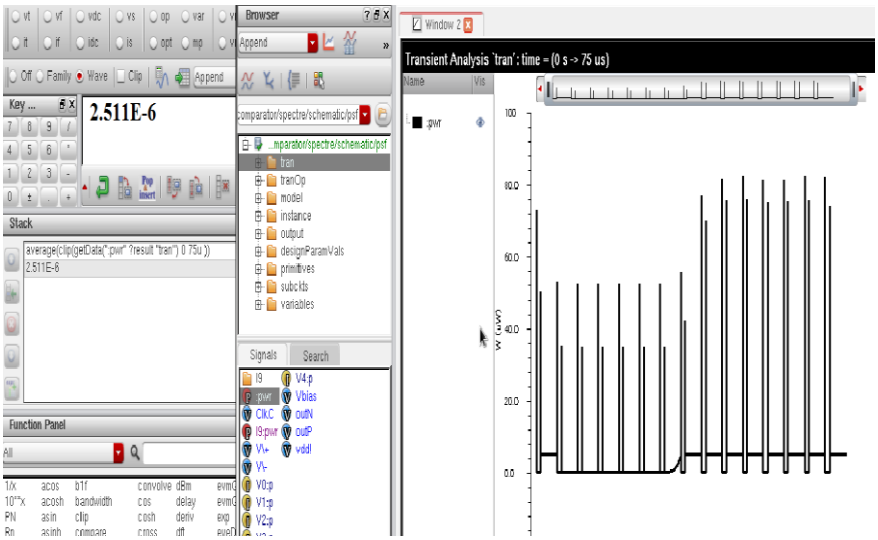

Figure 6. Power waveform after increasing the width of the MOSFETs

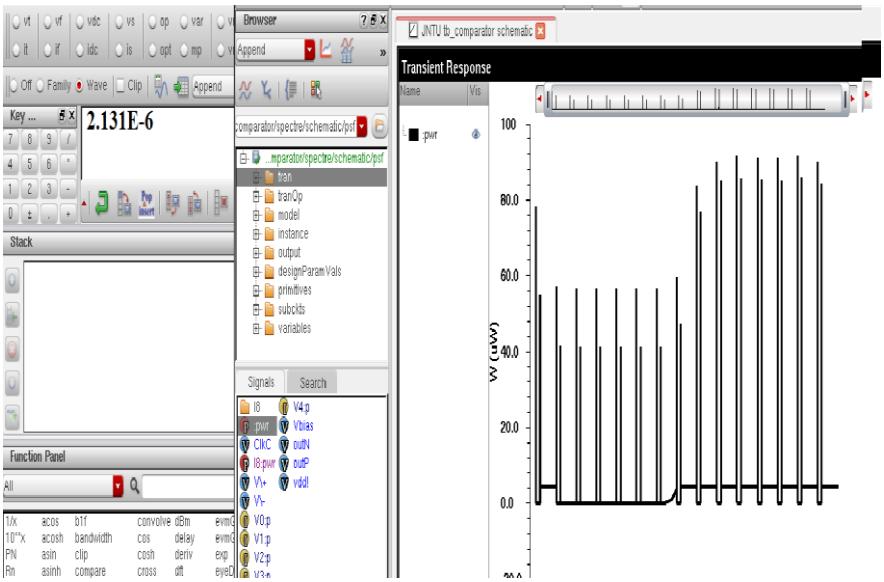

Figure 7. Power waveform after sizng the MOSFETs

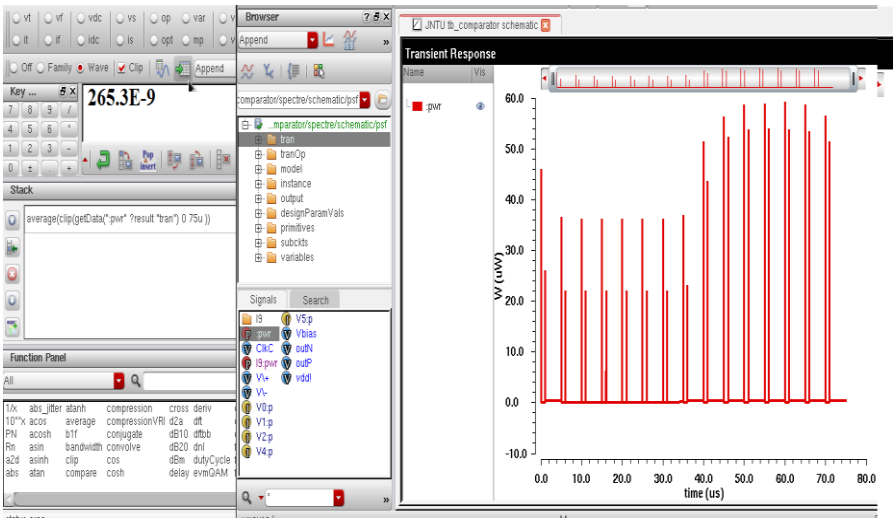

Figure 8. Power waveform after applying the HVt Cell concept

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The Dynamic Latch comparator average power consumption in 45nm technology is shown in Table-1. Increasing and sizing of the widths of MOSFETs, the power dissipation values are shown in table-1 and Figures 6&7.The average power dissipation was reduced from 2.5µW to 2.13µW respectively. Still further reducing the power HV_t(High V_t) concept was implemented in all the P-MOSFETs and the average power dissipation was reduced from 2.13µW to 265.3nW respectively as shown in figure.8. The proposed Dynamic Latch comparator simulation results are shown in theFigure.9.Monte-carlo analysis for finding the width of MOSFET at less offset voltage is shown in figure.10.Table-3 summarizes the performance of comparators and gives comparison to reference [2] and [9]. The proposed dynamic comparator layout is shown in figure.11. This work is suitable for 10-bit SAR ADC using the monotonic switching procedure.

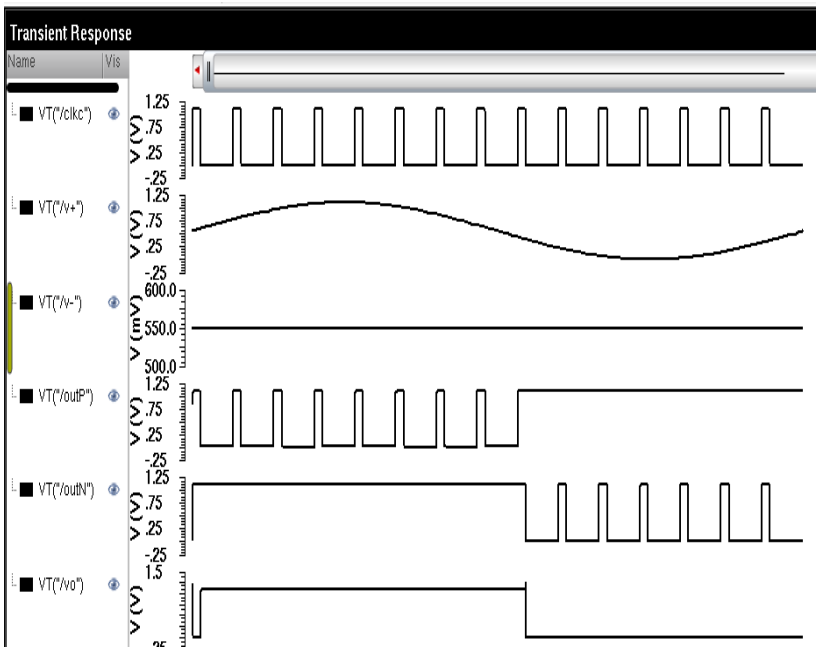

Figure 9. Simulation waveform of the proposed dynamic comparator

Table 3: Performance of Dynamic Comparator

Parameter	**ICSICT[9]2014**	**ICSICT[2]2010**	**Proposed Work**
Offset Voltage(V)	16m	19m	13m
Power(W)	--	50.4µ	2.131µ
Frequency(Hz)	3G	-	200K
Supply Voltage(V)	1.2	1.2	1.1

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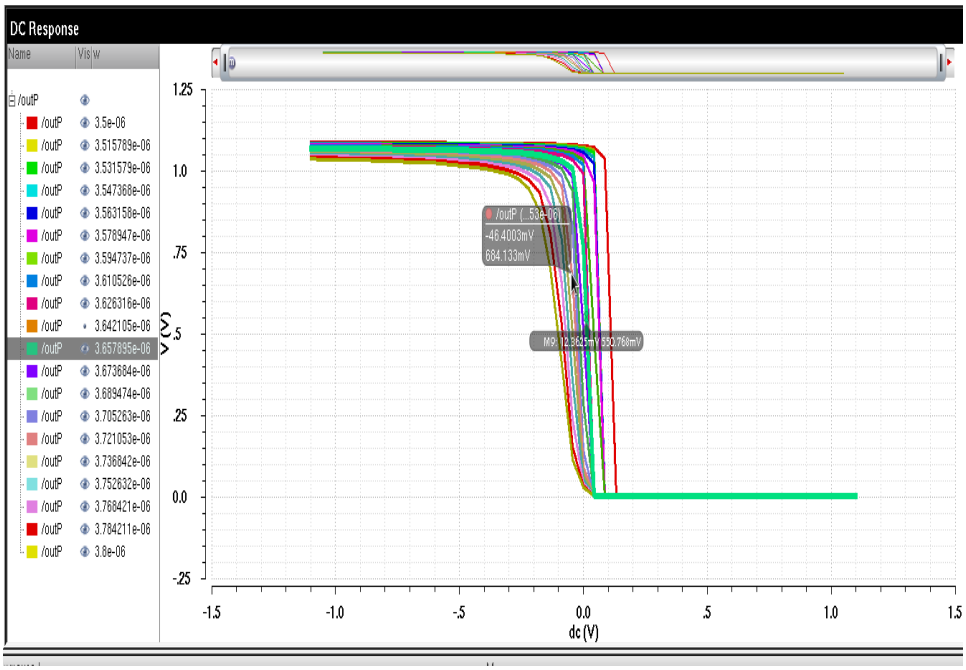

Figure 10. Monte-carlo analysis for less offset voltage

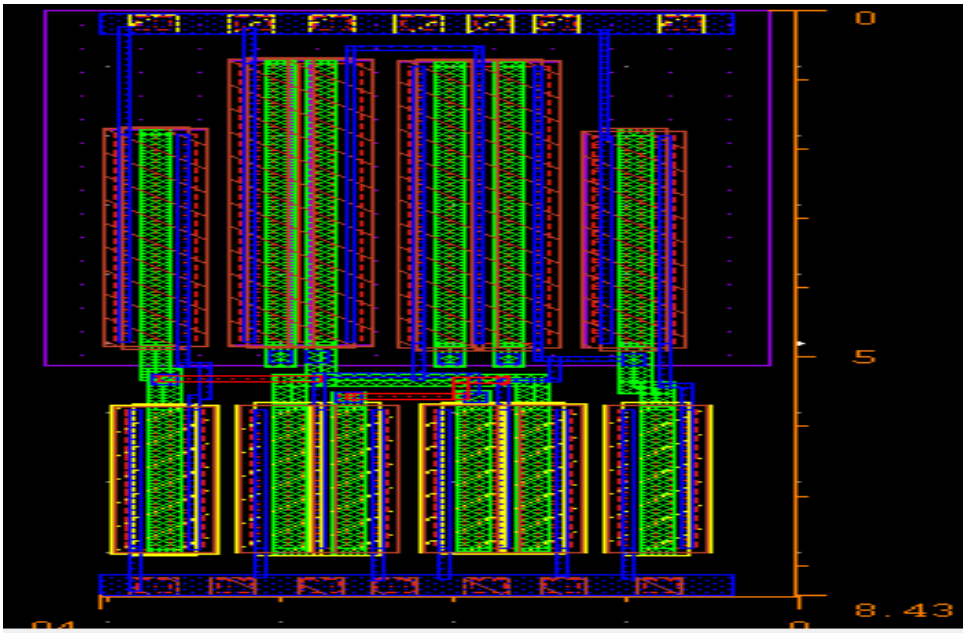

Figure 11. Layout of Praposed Dynamic Latch Comparator

Conclusion

Dynamic Latch comparator with Low offset and Low Power for SAR ADC using CMOS 45nm technology has been proposed. The Offset voltage of 13.0mV is achieved when matching the input differential pair transistors and the transistor M7. The Dynamic Latch comparator common mode voltages changing from -1.1V to 1.1V.The Dynamic Latch comparator power consumption was 2.13µW and further reduced to 265.3nW which can consider as ultra-low power because of HV_tCells implemented in all PMOS transistors. Initially, the delay is more later reduced to 342nS after matching the input transistors. Table-3 Summarizes the performance comparison between three comparators. The area of the comparator is $34.052(\mu m)^2$.Therefore the proposed comparator is more useful for less offset voltage and low power SAR ADC [7] in the 45nm CMOS Technology.

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